

## Re: iomapping a big endian area

**Source:** <http://linux.derkeiler.com/Mailing-Lists/Kernel/2005-04/1262.html>

---

**From:** James Bottomley (*James.Bottomley\_at\_SteelEye.com*)

**Date:** 04/05/05

To: Russell King <[rmk+lkml@arm.linux.org.uk](mailto:rmk+lkml@arm.linux.org.uk)>

Date: Tue, 05 Apr 2005 09:05:15 -0500

On Tue, 2005-04-05 at 08:42 +0100, Russell King wrote:

- > *Not so. There are two different styles of big endian. (Lets just face*
- > *it, BE is fucked in the head anyway...)*
- >
- > *physical bus: 31...24 23...16 15...8 7...0*
- >
- > *BE version 1 (word invariant)*
- > *byte access byte 0 byte 1 byte 2 byte 3*
- > *word access 31-24 23-16 15-8 7-0*
- >
- > *BE version 2 (byte invariant)*
- > *byte access byte 3 byte 2 byte 1 byte 0*
- > *word access 7-0 15-8 23-16 31-24*

These are just representations of the same thing. However, I did deliberately elect not to try to solve this problem in the accessors. I know all about the register relayout, because 53c700 has to do that on parisc.

However, I don't think it's the job of the io accessors to remap the register locations (primarily because the remapping depends on the documentation: a chip that's documented as BE on BE has no remapping required. Hoever, the same chip on LE would need this).

> *And guess which architecture implements \*both\* of these... Grumble.*

We have this in parisc too ...

James

—

To unsubscribe from this list: send the line "unsubscribe linux-kernel" in the body of a message to [majordomo@vger.kernel.org](mailto:majordomo@vger.kernel.org)

More majordomo info at <http://vger.kernel.org/majordomo-info.html>

Please read the FAQ at <http://www.tux.org/lkml/>