

Re: intel x86 instruction "cli"

Source: <http://linux.derkeiler.com/Newsgroups/comp.os.linux.development.system/2004-03/0375.html>

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Date: 03/19/04

Date: Fri, 19 Mar 2004 09:55:45 +0100

- > *In linux the ISR will mask the corresponding interrupt bit in PIC and*
- > *will call sti so that processor can identify any new interrupt*
- > *generation (as the interrupt*
- > *bit corresponding to the previous interrupt is cleared processor is*
- > *not notified*
- > *of the same interrupt again until ISR re enables that bit before*
- > *returning).*

I have a question on this. Why is the line masked, given that the hardware will not generate another int until it is serviced?
Why not just only acknowledge the PIC?

- > *The purpose of this is to service any higher priority interrupts*
- > *arrival during the execution of current interrupt's ISR.*

But if ints are enabled, lower priority interrupts could be triggered too, right?